NEW SCHEME

EC32

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Third Semester B.E. Degree Examination, January/February 2004

EC/TE/EE/ML/BM/IT/CS/IS

Electronic Circuits

Time: 3 hrs.] [Max.Marks : 100

Note: *1) Answer any FIVE questions.*
2) Each question carries equal marks.

1. (a) What do you understand by 'Diffusion capacitance'? Derive its expression. (6 Marks)

(b) Draw a double diode clipper, which limits at two independent levels and explain its operation. (6 Marks)

(c) Design a power supply using a FWR with capacitance filter to given an output voltage of 10V at 10mA from a 220V, 50Hz supply. The ripple factor must be less than 0.01. (8 Marks)

2. (a) What is a voltage multiplier circuit? Explain the operation of a full wave voltage doubler circuit. (6 Marks)

(b) Explain how a diode can be incorporated in a self bias circuit to compensate for

i) changes in V_{BE} ii) changes in I_{CBO} (6 Marks)

(c) Design a self bias transistor circuit for a stability of $s \leq 5$. The given data is as follows:

$$R_C = 1.6kr, \quad I_{CQ} = 3mA, \quad V_{CEQ} = 5V,$$
$$\beta_{d.c} = 45, \quad V_{cc} = 12V, \quad V_{BE} = 500mV$$

(8 Marks)

3. (a) Draw the hybrid model of a transistor and explain the significance of each element. (6 Marks)

(b) The hybrid parameters for a transistor used in the CE configuration are $h_{ie} = 1.5kr$, $h_{re} = 10^{-4}$, $h_{fe} = 70$ and $h_{oe} = 100\mu V$. The transistor has a load resistance of $1k\Omega$ and $R_s = 800\Omega$.Calculate

i) the current gain

ii) input resistance

iii) voltage gain and

iv) output resistance for the CE configuration. (8 Marks)

(c) State and prove Miller's theorem. (6 Marks)

4. (a) Draw the small signal high frequency CE model for a transistor and explain the significance of each component in the model. (5 Marks)

(b) Derive an expression for transistor trans conductance g_m and input conductance $g_{b'e}$ (10 Marks)

Contd.... 2

(c) Classify the various transistor amplifiers. (5 Marks)

5. (a) With a neat sketch, describe the concept of feedback in amplifier. (5 Marks)

(b) Using the block diagram approach, derive an expression for

i) input impedance of voltage series feedback amplifier. (5 Marks)

ii) output impedance of current shunt feedback amplifier. (5 Marks)

(c) If an amplifier has a bandwidth of 200kHz and a voltage gain of 100, what will be the new bandwidth and gain if 5% negative feedback is introduced. What is the product of gain and bandwidth before and after adding negative feedback? What should be the amount of feedback if the bandwidth is restricted to 1MHz? (5 Marks)

6. (a) Draw the circuit diagram and explain the operation with relevant waveforms of a class B push pull amplifier. Also show that the maximum conversion efficiency of the class B push pull amplifier is 78.5%. (12 Marks)

(b) A single transistor amplifier with transformer coupled load produces harmonic amplitudes in the output as

$$B_0 = 1.5mA \quad B_3 = 4mA$$
$$B_1 = 120mA \quad B_4 = 2mA$$
$$B_2 = 10mA \quad B_5 = 1mA$$

i) Determine the percentage total harmonic distortion.

ii) Assume a 2^{nd} identical transistor is used along with a suitable transformer to provide push pull operation. Use the above harmonic amplitudes to determine the new total harmonic distortion. (8 Marks)

7. (a) Define the following terms w.r.t op.amp

i) C.M.R.R

ii) Input offset current

iii) P.S.R.R

iv) Slew rate (4 Marks)

(b) Draw the circuit of a differential instrumentation amplifier using a transducer bridge and explain its features. Also derive the expression for its output voltage. (10 Marks)

(c) Design an op amp schmitt trigger circuit with $L.T.P = 2V$, $U.T.P = 4V$ and $V_{sat} = V_{0(max)} = \pm 10V$ (6 Marks)

8. (a) With neat circuit diagram, explain the working of successive approximation type of ADC. (7 Marks)

(b) Explain the operation of positive peak detector with relevant waveforms. (5 Marks)

(c) Draw the circuit diagram of Astable multi vibrator using 555 timer and explain its operation. (8 Marks)

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